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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 15

Application Number: 09/836,204
Filing Date: April 18, 2001
Appellant(s): SHIN, SEONG CHEOL

David C. Oren
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on March 30, 2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1-12 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,995,069	Tokunaga et al	11/1999
6,229,516	Kim et al	5/2001

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tokunaga et al(5,995,069) in view of Kim et al(6,229,516).

Tokunaga et al teach a method for driving a plasma display comprising the steps of: applying an upper driving signal(D1-D12) to address electrode lines provided at the upper block and applying a lower driving signal(D--D12) to address electrode lines provided at the lower block to overlap with the upper driving signal(simultaneous with the lower driving signal(see figures 9, 11; column 9, lines 58-68 and column 10, lines 1-12).

Tokunaga et al fail to drive a plasma display panel utilizing an asymmetry sustaining.

Kim et al teach a asymmetry driving method for driving a flat panel display(see figures 2, 9 and column 8, lines 6-19). It would have been obvious to have modified Tokunaga et al with the teaching of Kim, so as to improve the image quality(see Kim's column 9, lines 64-68); and since Kim has disclosed a plasma display is a flat panel display and the flat panel display could be either using a symmetry driving method(see figure 8) or an asymmetry driving method(see figure 9)(see figures 2, 8-9; column 1, lines 10-18; column 7, lines 22-68 and column 8, lines 1-19) and Tokunaga et al have disclosed the upper scanning driver(32a) and the lower scanning driver(32b) could be independently operated by themselves(see figure 10) and the upper data driver(34a)

and the lower data driver(34b) could be independently operated by themselves(see figure 11).

As to claims 8-11, Kim et al teach a driving apparatus having a controller(100) for controlling the energy recovery circuit(12, 14) and Kim et al teaches first and second signal for controlling first and second address drivers(12, 14) having different phase(delay)(see figures 2 and 9).

As to claims 2 and 11, Kim et al teach the lower driving signal(down A) is applied at halftime of an application period of the upper driving signal(see figure 9).

As to claims 3-6, Kim et al teach when the upper driving signal(up A) falls into ground level, the lower driving signal(down A) remains at a stable voltage level; when the lower driving signal(down A) falls into ground level, the upper driving signal(up A) remains at a stable voltage level (see figures 9, 12).

As to claim 12, Tokunaga et al teach a first scanning/sustaining driver(32A); a second scanning/sustaining driver(32B) and a common sustaining driver(33)(see figures 10-11).

(11) Response to Argument

Appellant argues that there is no suggestion of how Tokunaga's plasma display panel may be modified such that data is output by data driver based on start signals(STV1, STV2) on page 9. With Kim's teaching(see figures 2, 9, 12), Tokunaga can output upper data from the upper data driver(34a) and lower data from a lower data driver(34b) based on control signals(e.g. STV1 or STV2) since the lower data driver(34b) could be independently operated from the up data driver(34a).

Appellant argues that no indication that the plasma display panels utilize asymmetry on pages 7-9. Kim teaches an asymmetry drive method using in an LCD display(see figures 2, 9, 12). However, a plasma display and an LCD display are both dot matrix displays and they both need data(addressing) drivers and scanning drivers for applying data signals and scanning signals to the displays. If an asymmetry drive method could applied in data driver of an LCD display, so does in a plasma display. Kim gives an asymmetry driving method example for an LCD since LCD display are representatives of flat panel displays which include a plasma display field emission displays and electroluminescences display(see column 1, lines 5-18).

Appellant argues that Tokunaga and Kim do not suggest the claimed phase difference to each the first and second address drivers or an energy recovery circuit on pages 10 and 12. The examiner disagrees with that since Tokunaga teaches a first and second address drivers(34a, 34b) or energy recovery circuit(see figure 11) and Kim teach a first and second data drivers or energy recovery circuit(12, 14) having phase difference(up A, down A; up B and down B) from each other(see figures 2, 9, 12). Therefore, the combination of Tokunaga and Kim teach phase difference to each the first and second address drivers.

Appellant argues that Kim does not teach the lower driving signal is applied at an approximately halftime of an application period of the upper driving signal on a plasma display on pages 10-11 and 13. Kim teach the lower driving signal(down A or down B) is applied at an approximately halftime of an application period of the upper driving signal(up A or up B) on an LCD display(see figures 2, 9 and column 8, lines 23-28).

However, a plasma display and an LCD display are both dot matrix displays and they both need data(addressing) drivers for applying data signal to upper panel and lower panel. If the lower driving signal(down A or down B) can applied at an approximately halftime of an application period of the upper driving signal(up A or up B) on an LCD display, so does in a plasma display.

Appellant argues that Kim does not teach a period when the upper driving signal falls into a ground potential overlaps with a period when the lower driving signal remains at a stable voltage level and a period when the lower driving signal falls into a ground potential overlaps with a period when the upper driving signal remains at a stable voltage level on page 11. The examiner disagrees with that since Kim teach such features(see figures 9 and 12).

Appellant argues that Kim does not teach a data at the lower block is supplied at the period when the lower driving signal remains at a stable voltage level and a data at the upper block is supplied at the period when the upper driving signal remains at a stable voltage level on page 11. The examiner disagrees with that since Kim teach such features(see figures 9 and 12).

Appellant state that the examiner does not address driving an energy recovery circuit at the application time of the driving signal to raise the driving signals into a stable voltage level and driving the energy recovery circuit after the data was supplied to the corresponding block, thereby falling the driving signals into a ground voltage level on page 12. However, the examiner has point out the energy recovery circuit(12, 14)(Kim's display) on the final office action. Actually, both Tokumaga et al and Kim

teach driving an energy recovery circuit(34a, 34b in Tokumaga's display and 12, 14 Kim's display) in at the application time of the driving signal to raise the driving signals into a stable voltage level and driving the energy recovery circuit after the data was supplied to the corresponding block, thereby falling the driving signals into a ground voltage level(see Tokumaga's figures 9, 11, 12 and Kim's figures 2, 9).

Appellant state that the examiner does not addresses signals for driving the energy recovery circuit have a phase difference between the upper block and the lower block on page 12. However, the examiner has addressed such limitation on the final rejection(see claim 8 rejection above).

Appellant argues that Kim does not teach a controller(100) generating first and second control signals or delay provided between the controller and the second address driver, for delaying the second control signal on page 13. Even though Kim does not point out the controller(100) generating the first and second control signals and delay a second control signals, it is understandable the controller(100) generating the first and second control signals(delay signal) since the upper data driver(12) needs a first control signal and the lower data driver(14) needs a second control signal(delay signal) so the lower driver(14) can output lower data after the upper driver(12) output the upper data(see figures 2, 9, 12).

Appellant argues that Tokunaga does not teach first scanning/sustaining driver for upper block, a second scanning/sustaining driver for lower block and a common sustaining driver for driving common sustaining electrode lines included in the upper and lower blocks on page 13. The examiner disagrees with that since Tokunaga teach

first scanning/sustaining driver(32a) for upper block, a second scanning/sustaining driver(32b) for lower block and a common sustaining driver(33) for driving common sustaining electrode lines included in the upper and lower blocks(see figures 10-11).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Lun-yi, Lao

Lun-Yi Lao
Primary Examiner

May 1, 2004

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